

## CLAIMS

1. A delay locked loop comprising a line of delay cells (R1, R2, ..., Rn) mounted in series, a delay signal output by the loop being output from the output of one of the delay cells, the input of the delay cells line being connected to a first input of a phase/frequency detector (1), for which a second input is connected to an output from the delay cell, characterised in that the loop comprises control means (4, 7) capable of modifying the output from the delay cell connected to the second input of the phase/frequency detector (1), at the rate of a clock signal (H) when stimulated by control information (I).

2. Delay locked loop according to claim 1, characterised in that the control means comprise multiplexing means (4) with n inputs and one output, each input of the multiplexing means (4) being connected to one different delay cell output, the output from the multiplexing means being connected to the second input of the phase/frequency detector.

3. Phased locked loop according to claim 2, characterised in that the multiplexing means (4) comprise a multiplexer (5) and a sigma delta modulator (6) with a clock input on which said clock signal (H) is applied and a signal input on which said control information (I) is applied, the sigma delta modulator (6) outputting a digital control signal applied to the multiplexer (5).

4. Delay locked loop according to claim 1, characterised in that the control means comprise a first set of switches Iqi ( $i = 1, 2, \dots, n$ ), a second set of switches Ipi ( $i = 1, 2, \dots, n$ )

and a control circuit (7) with a clock input on which said clock signal (H) is applied and a control input on which said control information (I) is applied, the switch  $I_{pi}$  being placed at the output from the rank  $i$  delay cell  $R_i$  and the switch  $I_{qi}$  being placed in parallel with the assembly formed by the rank  $i$  delay cell  $R_i$  and the switch  $I_{pi}$ , switches  $I_{pi}$  and  $I_{qi}$  being controlled by control signals  $p_i$  and  $q_i$  respectively output from the control circuit (7).

5. Delay locked loop according to claim 4, characterised in that switches and switchable loads are placed at the input and output of the different delay cells ( $R_1, R_2, \dots, R_n$ ) such that the total number of switches used in the loop during operation of the loop is always the same, and each delay cell always sees the same load on its input and on its output.

6. Delay locked loop according to either claim 4 or 5, characterised in that the control circuit (7) comprises a sigma delta modulator with a clock input on which said clock signal (H) is applied and a signal input on which said control signal (I) is applied and a digital control circuit on which a digital control signal output by the sigma delta modulator is applied.

7. Delay locked loop according to claim 1, characterised in that the control information (I) is a fractional value  $p/q$  such that the output from the delay line is composed of the output from the rank  $n-1$  delay line for  $p$  clock ticks and the output from the rank  $n$  delay line during  $q$  clock ticks, where  $p$  and  $q$  are two integer numbers and  $q$  is greater than  $p$ , and the value of the delay of a delay cell is given by the relation:

$$\Delta t = q T / (qn - p),$$

where T is the period of a signal applied to the input of the delay line.

5           8. Delay locked loop according to claim 1, characterised in that the clock signal (H) is identical to a signal applied to the first input of the phase/frequency detector (1), except for a delay.

10           9. Delay locked loop according to claim 1, characterised in that the clock signal (H) is a signal with a period less than the period of the signal applied to the first input of the phase/frequency detector (1).

15           10. Delay locked loop according to claim 1, characterised in that it comprises means (8, 9, 10) to select a number of delay cells such that the loop will not get locked, during a loop latching phase.

20           11. Delay locked loop according to claim 10, characterised in that the means (8, 9, 10) provided to select the number of delay cells to prevent the loop from getting locked, during a loop latching phase, comprise a convergence analysis device (8), a switch (9) and a processing circuit (10), the input to the convergence analysis device (8) being connected to the output from the phase/frequency detector (1), the switch (9) being controlled such that the output from the

convergence device (8) is connected to the input to the processing circuit (10), the output from the processing circuit (10) being connected to a control input of the control means (4, 7).

12. Delay locked loop according to either claim 10 or 11, characterised in that it  
5 comprises means (10) of memorising the selected number of delay cells.